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<u>L4</u>	706/15-44.ccls.		2865	<u>L4</u>
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<u>L2</u>	L1 and arithmetic and multiplexing and logic and shifter and different near bit near sizing and different phases		407565	<u>L2</u>
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1. Document ID: US 5263122 A

Using default format because multiple data bases are involved.

L5: Entry 1 of 3

File: USPT

Nov 16, 1993

US-PAT-NO: 5263122

DOCUMENT-IDENTIFIER: US 5263122 A

TITLE: Neural network architecture

DATE-ISSUED: November 16, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nunally; Patrick O.	Diamond Bar	CA		

US-CL-CURRENT: 706/41

[Full](#) [Title](#) [Citation](#) [Front](#) [Review](#) [Classification](#) [Date](#) [Reference](#) [Text](#) [Image](#) [Claims](#) [KMC](#) [Drawn D](#)

2. Document ID: US 5165010 A

L5: Entry 2 of 3

File: USPT

Nov 17, 1992

US-PAT-NO: 5165010

DOCUMENT-IDENTIFIER: US 5165010 A

TITLE: Information processing system

DATE-ISSUED: November 17, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Masuda; Noboru	Kokubunji			JP
Yasunaga; Moritoshi	Kawaguchi			JP
Yamada; Minoru	Hanno			JP
Masaki; Akira	Musashino			JP
Asai; Mitsuo	Kokubunji			JP
Hirai; Yuzo	Tsukuba			JP
Yagyu; Masayoshi	Kokubunji			JP
Hayashi; Takehisa	Kodaira			JP

Doi; Toshio
Ishibashi; Kenichi

Kokubunji
Kokubunji

JP
JP

US-CL-CURRENT: 706/42

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3. Document ID: US 5138695 A

L5: Entry 3 of 3

File: USPT

Aug 11, 1992

US-PAT-NO: 5138695

DOCUMENT-IDENTIFIER: US 5138695 A

** See image for Certificate of Correction **

TITLE: Systolic array image processing system

DATE-ISSUED: August 11, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Means; Robert W.	Rancho Santa Fe	CA		
Sklar; Horace J.	Escondido	CA		

US-CL-CURRENT: 706/41; 382/156, 382/278, 706/22

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<u>L6</u>	L5 and different near (bit-sizes or bit near sizes)		0	<u>L6</u>
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<u>L3</u>	L1 and arithmetic and multiplexing and logic and shifter		0	<u>L3</u>
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<u>L10</u>		L9 same different near phases	0	<u>L10</u>
<u>L9</u>		different near (bit-sizes or bit near sizes)	73	<u>L9</u>
<u>L8</u>		arithmetic and multiplexing and logic and shifter and different near (bit-sizes or bit near sizes)	0	<u>L8</u>
<u>L7</u>		L1 and arithmetic and multiplexing and logic and shifter and different near (bit-sizes or bit near sizes)	0	<u>L7</u>
<u>L6</u>		L5 and different near (bit-sizes or bit near sizes)	0	<u>L6</u>
<u>L5</u>		L4 and arithmetic and multiplexing and logic and shifter	3	<u>L5</u>
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<u>L12</u>	L9 and different near phases		0	<u>L12</u>
<u>L11</u>	L9 and arithmetic and neural and weights		0	<u>L11</u>
<u>L10</u>	L9 same different near phases		0	<u>L10</u>
<u>L9</u>	different near (bit-sizes or bit near sizes)		73	<u>L9</u>
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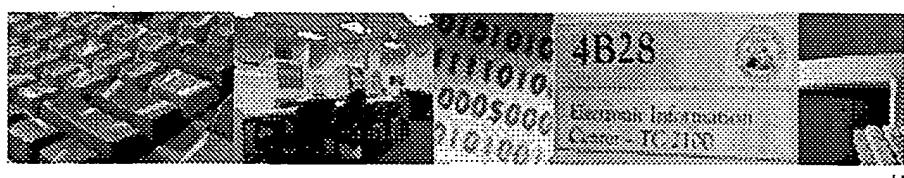
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1. **A bit-serial architecture for digital signal processing**
 Kanopoulos, N.;
Circuits and Systems, IEEE Transactions on
 Volume 32, Issue 3, Mar 1985 Page(s):289 - 291
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2. **BER floors due to heterodyne coherent crosstalk in space photonic switch networks**
 Blumenthal, D.J.; Granstrand, P.; Thylen, L.;
Photonics Technology Letters, IEEE
 Volume 8, Issue 2, Feb. 1996 Page(s):284 - 286
 Digital Object Identifier 10.1109/68.484268
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(328 KB\)](#) [IEEE JNL](#)
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3. **Digital phased array beamforming using single-bit delta-sigma converters and uniform oversampling**
 Kozak, M.; Karaman, M.;
Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on
 Volume 48, Issue 4, July 2001 Page(s):922 - 931
 Digital Object Identifier 10.1109/58.935709
[AbstractPlus](#) | [Full Text: PDF\(1684 KB\)](#) [IEEE JNL](#)
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4. **Visualization of radiation-pattern characteristics of phased arrays using corner shifters**
 Clenet, M.; Morin, G.A.;
Antennas and Propagation Magazine, IEEE
 Volume 45, Issue 2, April 2003 Page(s):20 - 35
 Digital Object Identifier 10.1109/MAP.2003.1203115
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5. **Blind equalization of turbo trellis-coded partial-response continuous-phase signaling over narrow-band Rician fading channels**
 Osman, O.; Ucan, O.N.;
Wireless Communications, IEEE Transactions on

Volume 4, Issue 2, March 2005 Page(s):397 - 403
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6. Design of good low-density parity-check codes for block fading channels

Xiaowei Jin; Eckford, A.W.; Fuja, T.E.;
[Military Communications Conference, 2004, MILCOM 2004, IEEE](#)
Volume 2, 31 Oct.-3 Nov. 2004 Page(s):1054 - 1059 Vol. 2
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7. Signal/Quantizing-distortion ratio measurements of fast-adaptive delta m systems

Eggermont, L.; Dijkmans, E.;
[Acoustics, Speech, and Signal Processing, IEEE International Conference on](#)
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8. Impact of SNR estimation error on turbo code with high-order modulation

Minying Sun; Yuan Li; Sumei Sun;
[Vehicular Technology Conference, 2004, VTC 2004-Spring, 2004 IEEE 59th](#)
Volume 3, 17-19 May 2004 Page(s):1320 - 1324 Vol.3
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9. On the baseband compensation of IQ imbalances in OFDM systems

Tarighat, A.; Sayed, A.H.;
[Acoustics, Speech, and Signal Processing, 2004, Proceedings. \(ICASSP '04\), International Conference on](#)
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10. Improved pre-combining group multiuser detection in BPSK-modulated systems with multiple receive antennas

Sfar, S.; Letaief, K.B.;
[Global Telecommunications Conference, 2003, GLOBECOM '03, IEEE](#)
Volume 1, 1-5 Dec. 2003 Page(s):267 - 271 Vol.1
Digital Object Identifier 10.1109/GLOCOM.2003.1258243

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11. Integrated 3-bit RF MEMS phase shifter with constant phase shift for active antennas in satellite broadcasting systems

Ko, Y.J.; Park, J.Y.; Bu, J.U.;
[TRANSDUCERS, Solid-State Sensors, Actuators and Microsystems, 12th International Conference on, 2003](#)
Volume 2, 8-12 June 2003 Page(s):1788 - 1791 vol.2

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12. Integrated photonic devices for fiber optic communication systems

Mason, B.; Ougazzaden, A.; Lenz, C.; Ketelsen, L.;
[Lasers and Electro-Optics Society, 2002, LEOS 2002, The 15th Annual Meeting](#)

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13. **Multiuser asynchronous SS/CDMA communication using dovetail constrained complex-valued spreading sequences**
Haspel, M.; Kalet, I.; Weiss, B.;
[Spread Spectrum Techniques and Applications, 2002 IEEE Seventh International Conference on](#)
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